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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,751	10/30/2003	Woogeun Rhee	YOR920030258US1	8750

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William E. Lewis
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,751	RHEE ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a reply to the Applicant's response on 03/10/2005. Claims 1-15 are presented in the instant application.

Upon reconsideration the finality of the rejection of the last Office action is withdrawn.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6 and 9-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson (U.S. Patent No. 6,122,336).

With respect to claims 1 and 9, Anderson discloses, in Figs. 4-5, a voltage-controlled delay line and its corresponding method comprising a delay element [404, 406, 408, 410]; and a phase interpolation circuit [412, 414] coupled to the delay element, wherein the delay element and the phase interpolation circuit are operative to (i) obtain an input signal and a complement of the input signal; and (ii) use the input signal [$A\phi_0$] and the complement of the input signal [$A\phi_4$] to perform a phase interpolation process so as to realize a complete delay timing range with respect to the input signal.

With respect to claims 2 and 10, Anderson discloses, in Figs. 4-5, that the phase interpolation process is a second-order phase interpolation process.

With respect to claims 3 and 11, Anderson discloses, in Figs. 4-5, that the delay tuning range is equivalent to 180 degrees of a period of the input signal (*according to inputs* $A\phi_0$ and $A\phi_4$, see Fig. 5).

With respect to claims 4 and 12, Anderson discloses, that the delay tuning range is guaranteed over a process variation.

With respect to claims 5 and 13, Anderson discloses, that the delay timing range is guaranteed over a temperature variation.

With respect to claims 6 and 14, Anderson discloses, in Fig. 4, that the complement of the input signal [$A\phi_4$] is used to generate an absolute 180-degree phase reference *(inverted)*.

3. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Garlepp et al. (U.S. Patent No. 6,133,773).

With respect to claim 15, Garlepp et al. discloses, in Figs. 6 and 7, an apparatus for delaying an input signal comprising a memory [650]; and at least one processor coupled to the memory [650] and operative to (i) obtain an input signal [750] and a complement [760] of the input signal; and (ii) use the input signal [750] and the complement of the input signal [760] to perform a phase interpolation process [740] so as to realize a complete delay tuning range with respect to the input signal.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (U.S. Patent No. 6,122,336) in view of Kim et al. (U.S. Patent No. 6,295,328).

With respect to claim 7, Anderson discloses, in Fig. 3 and 4, a delay-locked loop circuit comprising a voltage-controlled delay line comprising: (i) a delay element [404, 406, 408, 410], and (ii) a phase interpolation circuit [412, 414] coupled to the delay element; wherein the delay element and the phase interpolation circuit [412, 414] are operative to obtain an input signal and a complement of the input signal; and use the input signal [$A\phi_0$] and the complement [$A\phi_4$] of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal;

Anderson fails to disclose a phase detector being coupled to the voltage-controlled delay line for generating an error signal for adjusting a phase shift associated with the voltage-controlled delay line.

Kim et al. discloses, Fig. 4, a delay locked loop having a phase detector [30] coupled to a voltage-controlled delay line [32] for generating an error signal *(output of 30)* for adjusting a phase shift associated with the voltage-controlled delay line.

To configure the circuit of Anderson et al. with a phase detector as taught by Kim et al. to provide a clock generator with simplified construction and high operational safety would have been obvious to one of ordinary skill in the art at the time of the invention since Kim et al. teaches that such configuration would facilitate design simplicity and safety enhancement *(see Kim et al., col. 3, lines 26-27).*

With respect to claim 8, Anderson discloses, in Fig. 3 and 4, a clock and data recovery circuit comprising a) a clock recovery circuit [300, 308]; b) a voltage-controlled delay line comprising: (i) a delay element [404, 406, 408, 410], and (ii) a phase interpolation circuit [412, 414] coupled to the delay element; wherein the delay element and the phase interpolation circuit [412, 414] are operative to obtain an input signal and a complement of the input signal; and use the input signal [$A\phi_0$] and the complement [$A\phi_4$] of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal.

Anderson fails to disclose a data recovery circuit coupled to the voltage-controlled delay line for recovering data in accordance with a clock signal received from the voltage-controlled delay line.

Kim et al. discloses, Fig. 4, a data recovery circuit [33, 34, 35] being coupled to the voltage-controlled delay line for recovering data in accordance with a clock signal received from the voltage-controlled delay line.

To configure the circuit of Anderson et al. with a data recovery circuit as taught by Kim et al. to provide a clock generator with simplified construction and increased operational safety would have been obvious to one of ordinary skill in the art at the time of the invention since Kim et al. teaches that such configuration would facilitate design simplicity and safety enhancement *(see Kim et al., col. 3, lines 26-27).*

Remarks and Conclusion

6. Applicant's arguments filed 03/10/2005 have been fully considered but they are not persuasive.

With respect to the Applicant's argument on claims 1 and 9, at page 3, last paragraph, the Examiner disagrees with the Applicant's statements of a) "*First, Anderson does not disclose use of the input signal and the complement of the input signal to perform a phase interpolation process*" and b) "*Second, Anderson merely increases resolution of the frequency synthesizer by adding more clock phases. Anderson clearly does not provide a complete delay tuning range with respect to the input signal*". First, as clearly shown in Fig. 4 of Anderson, [$A\phi_0$] and [$A\phi_4$] are the input and the complement of the input signal inputted to the phase interpolators. Second, Anderson does provide a complete delay tuning range with respect to the input signal [$A\phi_0$] and the complement of the input signal [$A\phi_4$] the complement of the input signal via [412,414] the process of delaying and interpolating thus resulting in increasing resolution by adding more clock phases.

With respect to the Applicant's argument on claim 15, at page 4, third paragraph, the Examiner disagrees with the Applicant's statements of "*Garlepp does not use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal*". As clearly shown in Fig. 7 by Garlepp, delay circuit 685 is employed to provide a complete delay range of the input signal [750] and the complement of the input signal [760], which in turn inserted into phase interpolator [740].

With respect to the Applicant's argument regarding claims 7 and 8, at page 4, last paragraph, see response stated for claims 1 and 9 above since similar argument has been addressed for these two claims.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER